AMENDMENTS TO THE CLAIMS

Applicants submit below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently amended) A sense amplifier for nonvolatile memory cells comprising: a reference cell, a first load for connection between a supply terminal and an input terminal of an output comparator, said first load being connected to said reference cell via a first conduction terminal, and further comprising a second load, connectable to a nonvolatile memory cell, said first load and said second load each having a controllable resistance, and a control circuit controlling said first load and said second load and feeding said first load and said second load with a control voltage independent of an operating voltage between the first conduction terminal and a second conduction terminal of said first load,

wherein the first load is controlled by the control circuit in response to a voltage of the first conduction terminal of the first load to provide a reading current to the reference cell during a reading of the nonvolatile memory cell, wherein the reading current passes through both the reference cell and the first load at the same time.

2. (Original) The sense amplifier according to claim 1, wherein said control circuit comprises a feedback amplifier, connected to said first load, for controlling a voltage on said first conduction terminal.

3. (Original) The sense amplifier according to claim 2, wherein said feedback amplifier has a first input connected to said first conduction terminal of said first load, a second input connected to a voltage generator and supplying a constant reference voltage, and an output, connected to a control terminal of said first load.

4. (Original) The sense amplifier according to claim 1, wherein said first conduction terminal and said second conduction terminal of said first load are connected to said reference cell and, respectively, to a supply line, providing a supply voltage.

5. (Original) The sense amplifier according to claim 4, wherein said second load has a first conduction terminal, connectable to said memory cell, and a second conduction terminal, connected to said supply line.

6. (Original) The sense amplifier according to claim 5, wherein said first load and said second load comprise respective PMOS transistors and in that said respective first conduction terminals are drain terminals and said respective second conduction terminals are source terminals.

7. (Original) The sense amplifier according to claim 3, wherein said output of said feedback amplifier is connected to a control terminal of said second load.

8. (Original) The sense amplifier according to claim 1, comprising a first voltage limiter connected between said first load and said reference cell, for maintaining a drain terminal of said reference cell at a pre-determined voltage, and a second voltage limiter connectable between said second load and said memory cell for maintaining a drain terminal of said reference cell at said pre- determined voltage.

9. (Previously Presented) The sense amplifier according to claim 1, wherein said first conduction terminal of said first load is directly connected to said reference cell, and a first conduction terminal of said second load is directly connectable to said memory cell.

10. (Currently amended) The sense amplifier according to claim 9, comprising a voltage-regulator circuit associated with said first load for maintaining said first conduction terminal of said first load at a pre-set voltage.

11. (Original) The sense amplifier according to claim 1, comprising a comparator circuit having a first input and a second input connected to said first load and to said second load, respectively, and an output, supplying a signal correlated to a datum stored in said memory cell.

12. (Original) A nonvolatile memory comprising a plurality of memory cells and a read/write circuit, selectively connectable to said memory cells; wherein said read/write circuit comprises a plurality of sense amplifiers, according to claim 1.

13. (Currently amended) A sense amplifier for a memory cell, comprising:

a first transistor having a first conducting terminal coupled to a reference memory cell and a second conducting terminal for connection to a supply voltage; and

a control circuit coupled to a control input of the first transistor and the first conducting terminal of the first transistor such that the control circuit applies a control voltage to the control input of the first transistor in response to a voltage of the first conducting terminal, wherein the control circuit controls the first transistor to provide a reading current to the reference memory cell, wherein the reading current passes through both the reference memory cell and the first transistor at the same time.

14. (Previously presented) The sense amplifier of claim 13, wherein the control circuit comprises a first feedback amplifier.

15. (Previously presented) The sense amplifier of claim 14, wherein a first input of the feedback amplifier is coupled to a reference voltage.

16. (Previously presented) The sense amplifier of claim 15, wherein the reference voltage is a bandgap voltage.

17. (Previously presented) The sense amplifier of claim 14, wherein a second input of the first feedback amplifier is coupled to the first conducting terminal.

18. (Previously presented) The sense amplifier of claim 14, wherein an output of the first feedback amplifier is coupled to the control input of the first transistor.

19. (Previously presented) The sense amplifier of claim 13, wherein the first transistor is a PMOS transistor.

20. (Previously presented) The sense amplifier of claim 13, further comprising:

a comparator coupled to the first transistor and the memory cell for providing a voltage representative of data stored in the memory cell.

21. (Previously presented) The sense amplifier of claim 13, further comprising:

a second transistor having a first conducting terminal coupled to the memory cell.

22. (Previously presented) The sense amplifier of claim 21, wherein the second transistor has a second conducting terminal coupled to the supply voltage and a control input coupled to the control circuit.

23. (Previously presented) The sense amplifier of claim 21, wherein the control circuit comprises a first feedback amplifier coupled to the first transistor and a second feedback amplifier coupled to the second transistor.

24. (Previously presented) The sense amplifier of claim 23, wherein a first input of the second feedback amplifier is coupled to a reference voltage.

25. (Previously presented) The sense amplifier of claim 23, wherein a second input of the second feedback amplifier is coupled to the first conducting terminal of the second transistor.

26. (Previously presented) The sense amplifier of claim 23, further comprising:

a comparator;

wherein the first feedback amplifier and the second feedback amplifier are coupled to the comparator, which provides a voltage representative of data stored in the memory cell.

27. (Previously presented) The sense amplifier of claim 21, wherein the control circuit comprises a first feedback amplifier coupled to the first transistor and the second transistor.

28. (Previously presented) The sense amplifier of claim 13, further comprising:

a third transistor;

wherein the reference memory cell is coupled to the first conducting terminal of the first transistor through the third transistor.

29. (Previously presented) The sense amplifier of claim 28, further comprising:

an inverter coupled to a gate and a conducting terminal of the third transistor.

30. (Previously presented) The sense amplifier of claim 13, wherein the supply voltage is less than or equal to about 1.5 volts.

31. (Previously presented) The sense amplifier of claim 30, wherein the supply voltage is less than 1.0 volts.

32. (Previously presented) The sense amplifier of claim 13, wherein the first transistor acts as a reference load.

33. (Previously presented) The sense amplifier of claim 13, wherein the control voltage is substantially independent of a voltage difference between the first and second conducting terminals.

34. (Previously presented) The sense amplifier of claim 13, wherein the control circuit controls the first transistor such that the first conducting terminal is maintained at a determined voltage that is less than the supply voltage.

35. (Previously presented) The sense amplifier of claim 34, wherein the determined voltage is within approximately 0.4 volts of the supply voltage.

36. (Previously presented) The sense amplifier of claim 13, wherein the first transistor is controlled to provide a reading current to the reference memory cell during a reading of the memory cell.